

MC74HC125A, MC74HC126A

Quad 3-State Noninverting Buffers

High-Performance Silicon-Gate CMOS

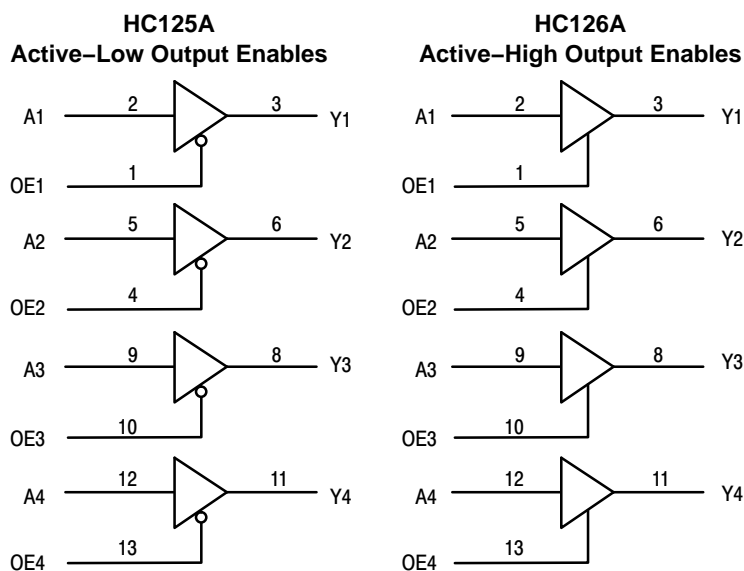
The MC74HC125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125A) or active-high (HC126A).

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND



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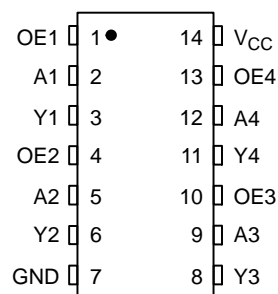


SOIC-14 NB
D SUFFIX
CASE 751A

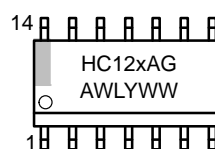


TSSOP-14
DT SUFFIX
CASE 948G

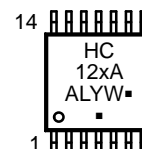
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

- x = 5, 6
- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| HC125A | | | HC126A | | |
|--------|--------|---|--------|--------|---|
| Inputs | Output | | Inputs | Output | |
| A | OE | Y | A | OE | Y |
| H | L | H | H | H | H |
| L | L | L | L | H | L |
| X | H | Z | X | L | Z |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74HC125A, MC74HC126A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 35 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C
TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|---|--------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | $V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0 | 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IH} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | 2.2 | |
| | | | 4.5 | 3.98 | 3.84 | 3.7 | |
| | | | 6.0 | 5.48 | 5.34 | 5.2 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IL} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | 0.4 | |
| | | | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | | 6.0 | 0.26 | 0.33 | 0.4 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4.0 | 40 | 160 | μA |

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|---|------------------|--------|---------|------|
| | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3) | 2.0 | 90 | 115 | 135 | ns |
| | | 3.0 | 36 | 45 | 60 | |
| | | 4.5 | 18 | 23 | 27 | |
| | | 6.0 | 15 | 20 | 23 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4) | 2.0 | 120 | 150 | 180 | ns |
| | | 3.0 | 45 | 60 | 80 | |
| | | 4.5 | 24 | 30 | 36 | |
| | | 6.0 | 20 | 26 | 31 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4) | 2.0 | 90 | 115 | 135 | ns |
| | | 3.0 | 36 | 45 | 60 | |
| | | 4.5 | 18 | 23 | 27 | |
| | | 6.0 | 15 | 20 | 23 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 22 | 28 | 34 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{in} | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |
| C _{out} | Maximum 3-State Output Capacitance (Output in High-Impedance State) | - | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF | |
| | | 30 | | | | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

MC74HC125A, MC74HC126A

SWITCHING WAVEFORMS

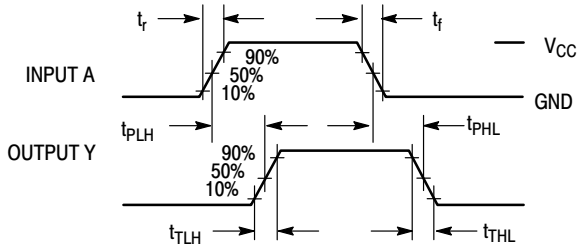


Figure 1.

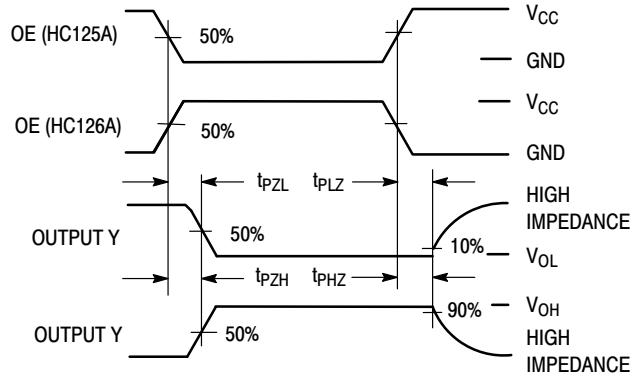
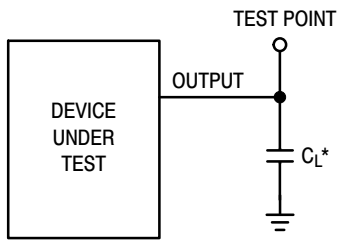
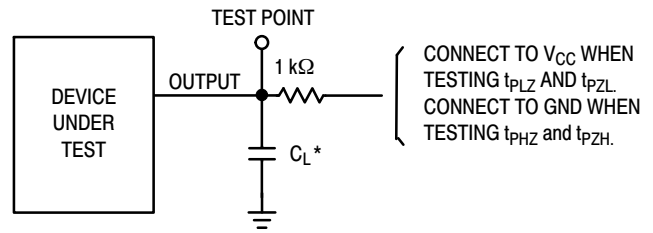


Figure 2.



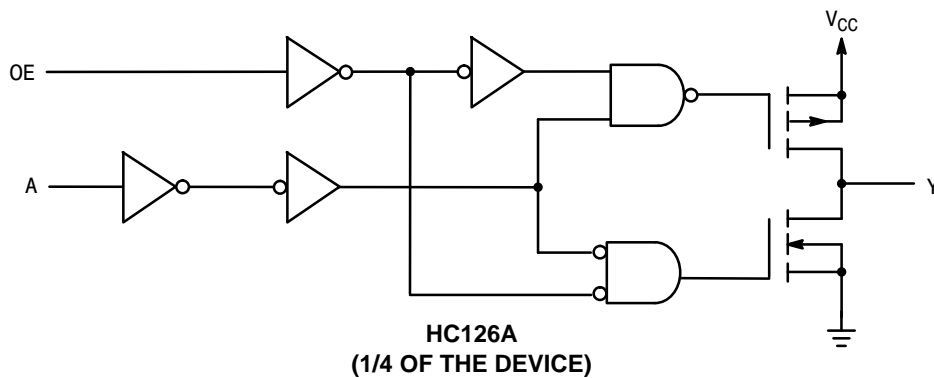
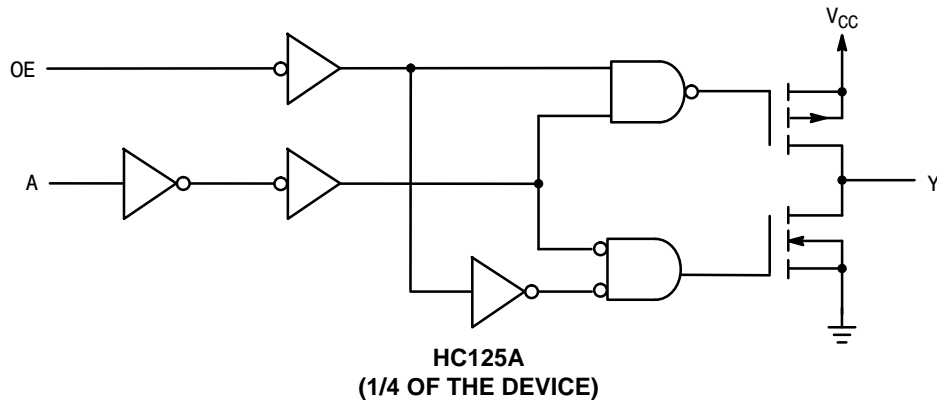
*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit



MC74HC125A, MC74HC126A

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------------|-------------------------|--------------------|
| MC74HC125ADG | SOIC-14 NB (Pb-Free) | 55 Units / Rail |
| MC74HC125ADR2G | SOIC-14 NB (Pb-Free) | 2500 / Tape & Reel |
| MC74HC125ADTG | TSSOP-14 (Pb-Free) | 96 Units / Rail |
| MC74HC125ADTR2G | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| MC74HC126ADG | SOIC-14 NB (Pb-Free) | 55 Units / Rail |
| MC74HC126ADR2G | SOIC-14 NB (Pb-Free) | 2500 / Tape & Reel |
| MC74HC126ADTR2G | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV74HC125ADG* | SOIC-14 NB (Pb-Free) | 55 Units / Rail |
| NLV74HC125ADR2G* | SOIC-14 NB (Pb-Free) | 2500 / Tape & Reel |
| NLV74HC125ADTG* | TSSOP-14 (Pb-Free) | 55 Units / Rail |
| NLV74HC125ADTR2G* | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV74HC126ADR2G* | SOIC-14 NB (Pb-Free) | 2500 / Tape & Reel |
| NLV74HC126ADTR2G* | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |

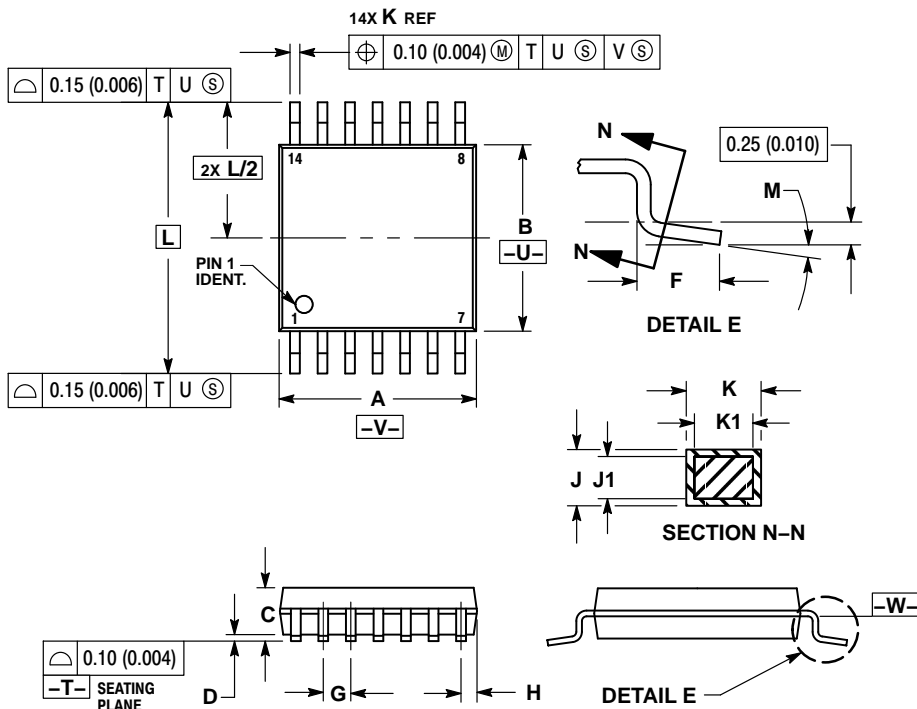
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MC74HC125A, MC74HC126A

PACKAGE DIMENSIONS

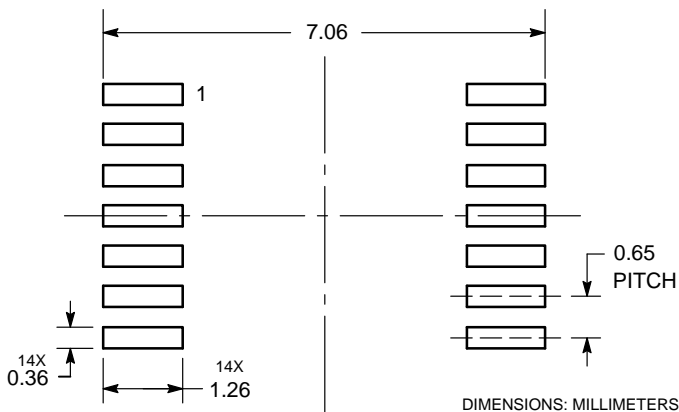
TSSOP-14
CASE 948G
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

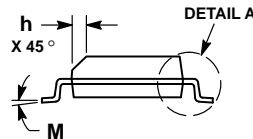
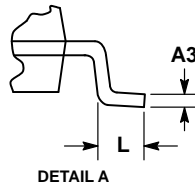
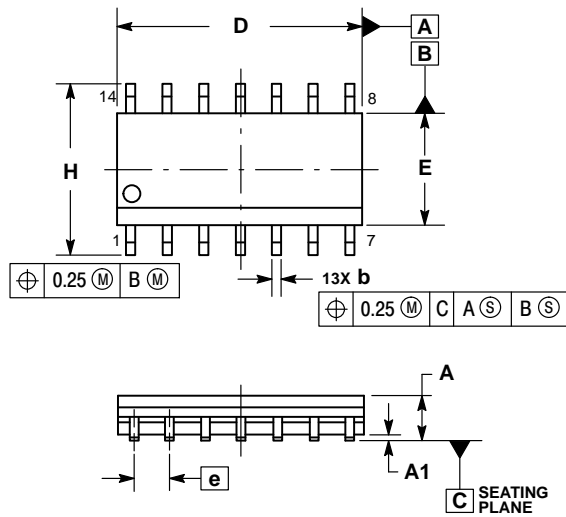


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC125A, MC74HC126A

PACKAGE DIMENSIONS

SOIC-14 NB
CASE 751A-03
ISSUE K

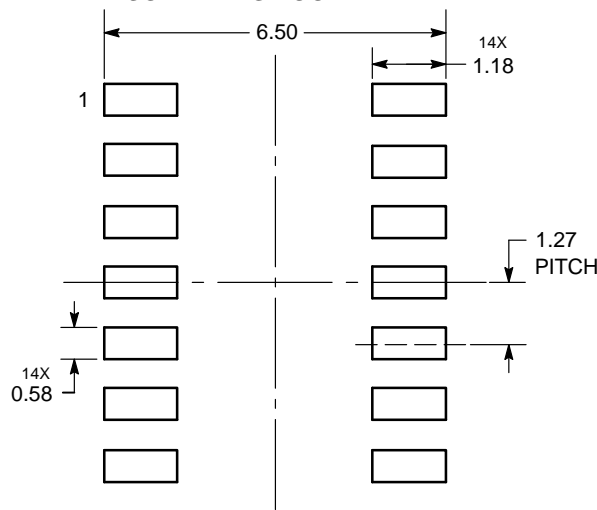


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.


| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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